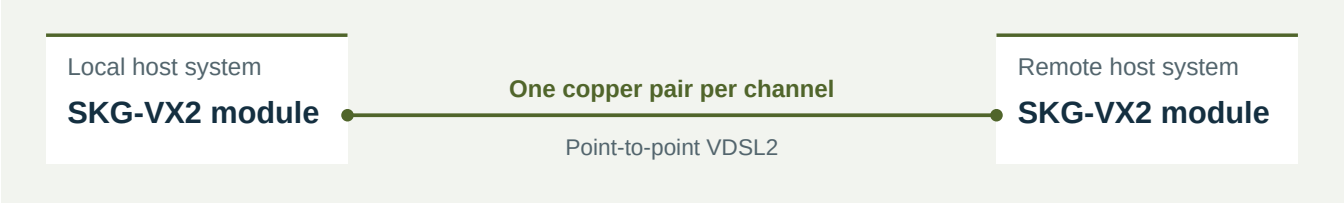
INDUSTRIAL NETWORKING / EMBEDDED MODULES

Embedded VDSL2 Ethernet Extenders

The SKG-VX2 family carries Ethernet traffic over existing copper pairs. A board at each end forms a point-to-point link. Two configurations serve single-link installations and multi-line equipment.



Model selection

Parameter	SKG-VX2-1	SKG-VX2-12
Independent DSL channels	1	12
Host Ethernet channels	1	12
Host bandwidth target	1 Gbit/s	12 Gbit/s transmit, 24 Gbit/s bidirectional (aggregate)
Estimated power per channel	4 W typical / 6 W peak	4 W typical / 6 W peak
Total board peak estimate	Board total pending measurement	Approximately 80 W including shared circuitry

Host bandwidth describes the board-to-host interface. DSL payload throughput depends on the copper link.

DSL link and reference performance

Profile 35b is supported. The design targets a reach of 2–3 km, with lower data rates on longer pairs. The figures below are preliminary reference values pending prototype measurements.

Copper pair length	Reference DSL payload throughput
1,000 m	36 Mbit/s
2,000 m	10 Mbit/s
3,000 m	2 Mbit/s

Cable gauge and electrical noise affect throughput. On the 12-channel board, crosstalk between active pairs reduces effective payload.

Link operation

Both endpoints use the same hardware. AUTO negotiates the CO/CPE roles over the copper pair. A host can also force the central-office (CO) or customer-premises (CPE) role in software through the CLI or web interface. Each channel operates independently without bonding or an external DSLAM.

Host integration and operating limits

Both variants are bare OEM boards. The integrator supplies the host motherboard and controller, system power and enclosure. All host interfaces use a board-to-board connector.

Electrical and environmental data

Parameter	Preliminary specification and integration notes
Input power	12–24 V DC proposed, supplied by the host. Final input tolerance, maximum current and power pins are pending hardware freeze.
Protection	On-board targets include overcurrent, overvoltage, overtemperature and ESD protection. The host supplies reverse-polarity and high-energy surge protection.
Fault isolation	Design target: a fault on one channel leaves the other channels running. Trip thresholds and fail-safe recovery remain to be defined.
Operating temperature	Target −40 °C to +75 °C. The chip is rated 0 °C to +70 °C. Cold start at −40 °C and full-load operation at +75 °C require prototype validation, particularly on the 12-channel board.
Relative humidity	5–95% RH, non-condensing.
Mechanical envelope	PCB dimensions, component height, mounting locations, connector position, keep-out zones and thermal clearance are pending mechanical design completion.

Host interface and start-up

Ethernet interface. Target SGMII, QSGMII or 1000BASE-X interfaces require external circuitry. A direct connection to a host PHY is an alternative subject to hardware validation. The board has no RJ45 or optical port.

Host control. Both host controllers must agree on DSL signal levels before the DSL circuitry starts. After each boot the host reissues service configuration via the CLI or web interface. The module stores no persistent local boot configuration. SSH and Telnet are supported for configuration and monitoring.

Power validation. Inrush magnitude and duration, idle, training and full-traffic consumption across temperature are pending measurement. The 12-channel test must include simultaneous training and traffic. Power sequencing, undervoltage and power-off behavior are to be finalized.

EMC integration

MIL-STD-461G is the end-equipment design target. Final system-level compliance is the integrator’s responsibility. Board protection references are IEC 61000-4-2 (ESD), IEC 61000-4-4 (EFT) and IEC 61000-4-5 (surge). Board-level test results and multi-channel grounding, filtering and shielding guidance are pending validation.

Preliminary V0.1. For project evaluation. Power, throughput and environmental targets remain subject to prototype validation. The final released datasheet will govern after hardware freeze.